Ultra low power voltage regulator with power-on-reset
(ULPRegPOR1)

Description
This is a special ultra-low power linear voltage regulator with power on reset functionality. It is specially designed for low power battery applications, where the nominal battery voltage does not correlate with the 0.25 µm thin-oxide transistor supply voltage.

The regulator is implemented in the MagnaChip 0.25 µm CMOS process HM25E with EEPROM option; it utilises the ‘super’ high voltage transistors and can therefore handle input voltages up to 5 V.

The built-in voltage bandgap reference makes it very stable towards supply voltage, temperature and process variations.

Features
- Ultra low supply current (<1 µA)
- Very accurate output voltage (bandgap stabilised)
- Temperature stable output voltage
- Power on reset circuit with static threshold levels (correlated with the bandgap)

Applications
- Supplying ‘low voltage’ circuits in ultra-low power battery applications
- Keeping data retention on RAM blocks in sleep mode
- Generating reliable power-on-reset in battery application (static reset threshold)

Technology
MagnaChip HM25E.
Portable to alternative CMOS technologies.
Proven in silicon

Schematic
For further information please contact us
asic@delta.dk
Pin list

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VddA</td>
<td>Analog</td>
<td>Positive power supply</td>
</tr>
<tr>
<td>Vout</td>
<td>Analog</td>
<td>Regulated output voltage</td>
</tr>
<tr>
<td>Rst</td>
<td>Out</td>
<td>Power-on-reset</td>
</tr>
<tr>
<td>RstNot</td>
<td>Out</td>
<td>Inverted power-on-reset</td>
</tr>
<tr>
<td>FBin</td>
<td>Analog</td>
<td>Feedback input (must be connected to Vout always)</td>
</tr>
<tr>
<td>VssA</td>
<td>Analog</td>
<td>Negative power supply</td>
</tr>
</tbody>
</table>

Electrical characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition/Note</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_th_up</td>
<td>Less than 100 mV/1s slope</td>
<td>2.07</td>
<td>2.12</td>
<td>2.16</td>
<td>V</td>
</tr>
<tr>
<td>V_th_down</td>
<td>Included 20 mV offset</td>
<td>1.94</td>
<td>1.99</td>
<td>2.02</td>
<td></td>
</tr>
<tr>
<td>V_hysteresis</td>
<td></td>
<td>0.11</td>
<td>0.13</td>
<td>0.16</td>
<td>mV</td>
</tr>
<tr>
<td>V_th_up</td>
<td>Mismatch Monte-Carlo, one sigma</td>
<td>36</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_th_down</td>
<td></td>
<td>32</td>
<td>32</td>
<td></td>
<td></td>
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<tr>
<td>V_hysteresis</td>
<td></td>
<td>8</td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage</td>
<td>Supply voltage 2.5 V-to-5.0 V</td>
<td>2.32</td>
<td>2.36</td>
<td>2.41</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Mismatch Monte-Carlo, one sigma</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LoopGain</td>
<td></td>
<td>55</td>
<td>60</td>
<td>61</td>
<td>dB</td>
</tr>
<tr>
<td>PhaseMargin</td>
<td>Cdigital_supply =1 µF, Iload = 5 nA</td>
<td>87</td>
<td>87</td>
<td></td>
<td>deg</td>
</tr>
<tr>
<td></td>
<td>Cdigital_supply =1 µF, Iload = 10 µA</td>
<td>69</td>
<td>77</td>
<td></td>
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</tr>
<tr>
<td>Isupply, static</td>
<td>Supply voltage 2.7 V-to-3.3 V</td>
<td>580</td>
<td>760</td>
<td>1000</td>
<td>nA</td>
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<tr>
<td></td>
<td>Supply voltage 2.5 V-to-5.0 V</td>
<td>570</td>
<td>1120</td>
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<tr>
<td>Supply voltage</td>
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<td>2.7</td>
<td>3.0</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>Extended sup. voltage</td>
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<td>2.5</td>
<td>5.0</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

Measurement

The ULPVregPOR1 has been tested in silicon. The measured performance complies very well with the simulated electrical characteristics. The output voltage variation on one lot has been measured to 23 mV (one sigma).