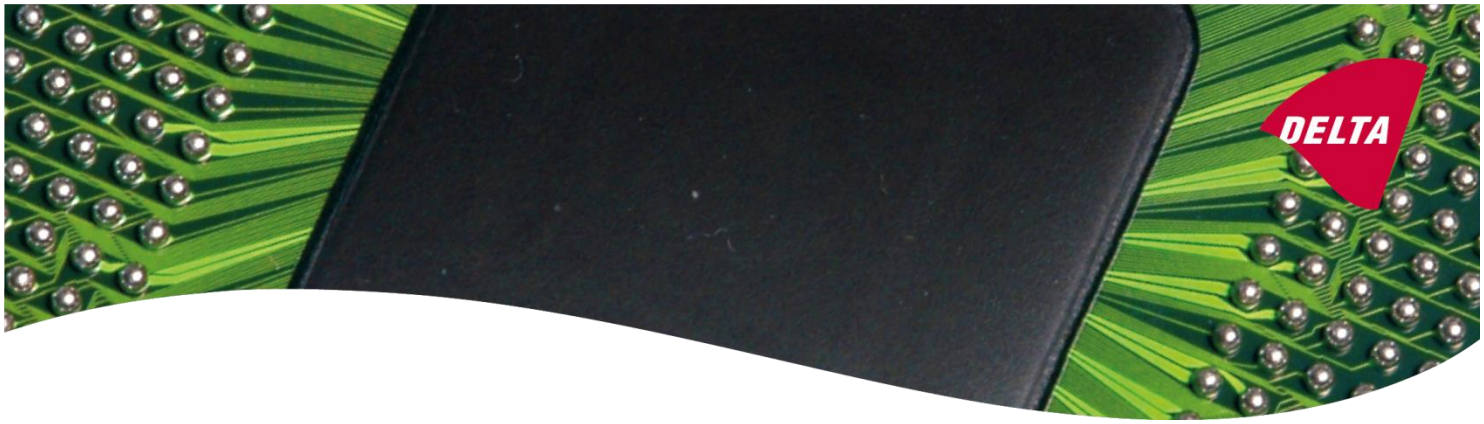

Toll road on-board unit device

Single chip front-end and baseband controller

Overview

DELTA has been working with toll road chips since 1984. Our single chip toll road device supports the GSS standard v.3.2. It consists of an analog part including an analog receiver frontend and a digital baseband controller and is used for Electronic Toll Collection (ETC)

It operates in two modes: Standby and active. In standby mode the device searches for a valid downlink from the Road Side Unit. In this mode only a limited part of the functionality is operational in order to reduce power consumption.
Active mode is entered when a valid downlink signal has been detected. When the device is in active mode it is fully operational and power to the baseband controller is enabled; the device is now ready to perform transactions with the Road Side Unit.

Below is a short description of the main functional blocks on the chip:

Low Noise Amplifier: Receives and amplifies the down converted downlink signal. The block has two operational modes: low power mode for downlink signal detection in standby mode and high power mode for receiving downlinks in active mode.

Voltage Regulator: Converts the external battery voltage to 1.8 V. The regulator has two modes, one low performance mode for powering the device in standby mode and one for active mode.

XTAL Oscillator: Ultra low power (ULP) crystal oscillator. This block is always active.

Wake-up Discriminator: Detects the 500 Kbit AM modulation on the 5.8 GHz carrier and search for a valid downlink signal. When found an interrupt is provided to the state controller. This block is always active.

State Controller: System state controller. By interrupt from the wake-up discriminator the controller activates the PLL and voltage regulator to power up of the baseband for active mode. The transition from active to standby is equally handled by this block. This block uses the 32 kHz clock and is always active.

Power-On Reset: This block monitors the regulated voltage level and asserts the main system reset if the voltage drops too low. This block is always active.

PLL: Multiplies the XTAL oscillator frequency of 32 kHz to 12 MHz for use in the baseband controller. This block is only powered in active mode.

HDLC: Takes care of sending/receiving and encoding/ decoding the HDLC (High-Level Data Link Control) frames. The FM0 encoded downlink bit stream is decoded and the validity of the frame is checked before the received data is transferred to a receive buffer (FIFO). Uplink data is taken from a buffer (FIFO) too and put into the HDLC frame structure before it is BPSK encoded with 1.5 or 2.0 MHz subcarrier for direct transmission over the antenna.

Encryption: 3DES is used for data encryption, but other encryption standards could also be implemented, e.g. AES.

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User Interface: Sound signals are generated using a configurable PWM (Pulse Width Modulator) so different frequencies can be produced. The output could be connected to a piezoelectric speaker. Support for various custom functions like push buttons and tamper detection can be implemented.

Timers: Used to obtain correct uplink timing and other general purpose timing tasks.

CPU: The microcontroller executes the firmware and makes mostly household tasks so an 8 bit processor has usually enough power to fulfil the requirements.

Serial Interface: This block contains a general purpose serial interface e.g. UART or SPI. For firmware implementation a CPU debug interface can be implemented which can be switched off for privacy reasons.

Power Management: Controls power-on and reset sequence (POR). For reducing power consumption, clock to various blocks can be switched off here.

Flash Memory: Contains the firmware and the tag specific data. This block an also be replaced by a ROM containing the firmware and a special RAM for the tag specific data which is powered even when the device is in standby mode.

Data RAM: General purpose memory for use with the CPU firmware execution.

Let us help

Get your own toll road chip !

For further information please contact us

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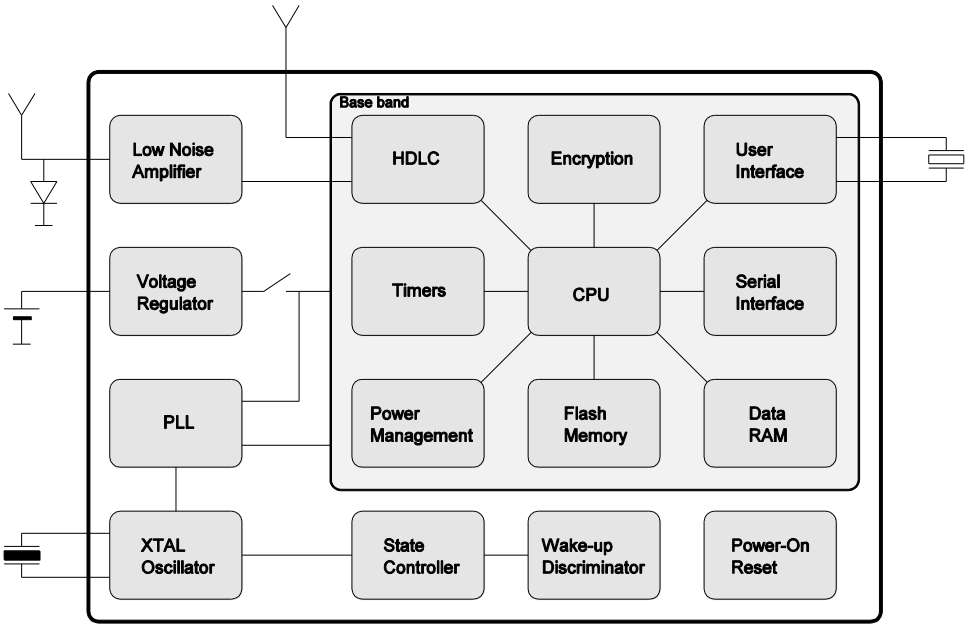

Key parameters		
Parameter	**Value**	**Note**
Supply voltage	2.0 – 3.6 V	Battery
Standby mode current	< 2.9 µA	Average while searching for downlink
Active mode current	< 4.0 mA	Fully operational (all blocks activated)
Start-up time	2.5 ms	Standby to active
Sensitivity	< 1.5 mVpp	Input signal to LNA