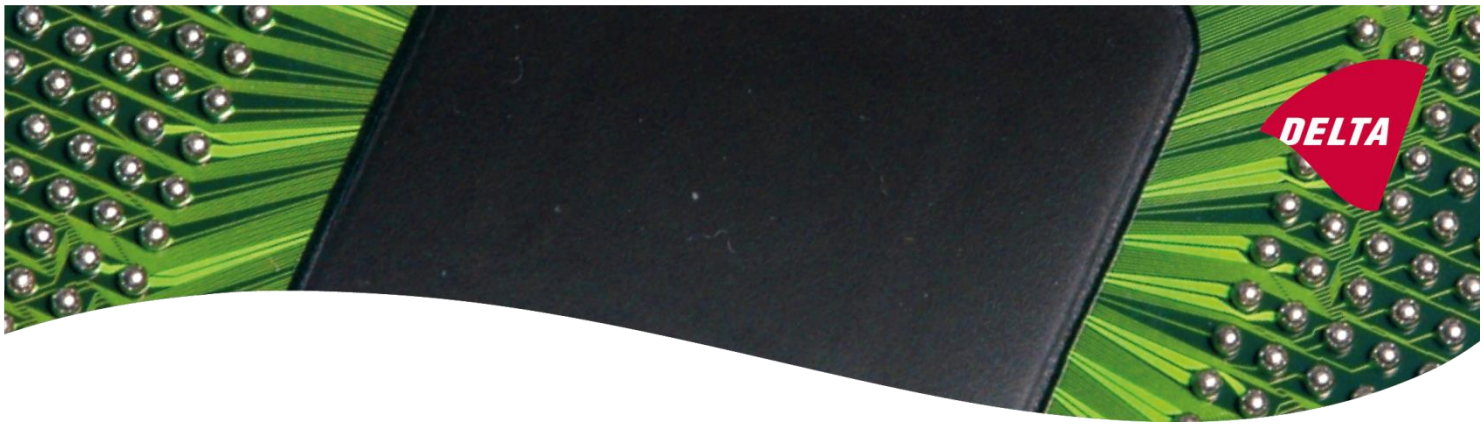


RFID analog front-end IP in 0.18 µm

Overview

DELTA has developed a contact-less RFID transceiver front-end for general purpose applications in the 13.56 MHz range ISO 14443A and ISO 15693.

Features

- Low power low voltage operation
- Contact-less power supply (on-chip full wave rectifier)
- Radio frequency 13.56 MHz inductive coupling
- Supports: Type A ASK 100% Miller, Type B ASK 10% NZR-L, etc.
- Edge sensitive demodulator with programmable threshold
- Carrier detector
- High power and soft load modulator for 'back-scatter' transmission
- 1.8 V voltage regulator with correlated power-on-reset
- PLL for 13.56 MHz clock generation at 100% modulation
- Clamp detector with programmable level (ex. inhibit EEPROM write operation until RF field is strong enough to support large supply current)
- Analog clamp current readout for prototype debugging and antenna calibration
- RC oscillator for watch-dog or other household application

Technology

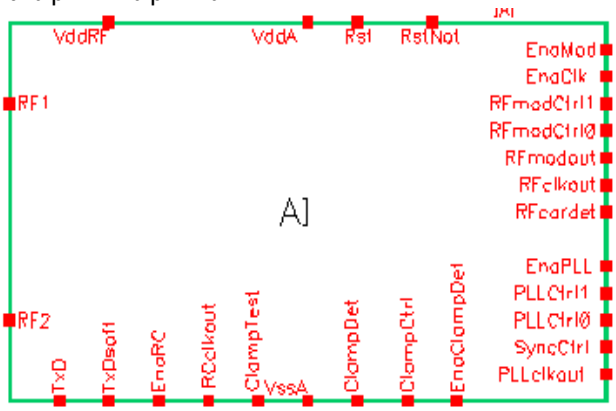
MagnaChip: HM18EW (Merged EEPROM), High resistive poly 10 kΩ/sq, MiM capacitors 1.5 fF/µm^2.
(Note: 3.3 V or 5.0 V transistor option NOT required)

Portable to other 180 nm CMOS with Schottky diodes.

Proven in silicon.

Dimensions

920 µm x 770 µm = 0.71 mm^2



For further information please contact us

asic@delta.dk

Pin list

Pin name	Type	Description
VddRF	Power	Positive supply (RF field, clamped to ~3.5 V, ext filter cap needed)
VssA	Power	Negative supply
VddA	Power	Positive supply (Regulated to 1.8 V, external filter cap needed)
RF1	Analog/Power	RF power-link, external coil and capacitor connection
RF2	Analog/Power	
Rst	Digital, output	Power-On-Reset, Active high (resetting)
RstNot	Digital, output	Power-On-Reset-Not, Active low (resetting)
EnaClampDet	Digital, input	Enable ClampDetect circuit, Active high
ClampCtrl	Digital, input	[0] => low clamp detect level , [1] = high clamp detect level
ClampDet	Digital, output	Status signal, [1] => clamping, [0] => no clamping
ClampTest	Analog, output	Fraction of internal clamp current for test (NMOS sink)
EnaMod	Digital, input	Enable RF modulator circuit, Active high
RFmodout	Digital, output	Modulation output, [0] => 'dark period', 0% modulation
EnaClk	Digital, input	Enable RF clock and carrier detector circuit, Active high
RFmodCtrl0	Digital, input	Control signal for RF modulator threshold [00]=low threshold (high sensitivity), [11]=high threshold (low sensitivity)
RFmodCtrl1	Digital, input	
RFclkout	Digital, output	Extracted RF carrier (Note: NOT valid in TxD and 'dark' periods)
RFcardet	Digital, output	Status signal, [1] => carrier, [0] => NO carrier 'dark period'
EnaPLL	Digital, input	Enable PLL, Active high (mainly for simulation)
PLLCtrl0	Digital, input	PLL frequency control, Default [01] => 13.56 MHz [00] => -20%, [10] => +20%, [11] => +40%
PLLCtrl1	Digital, input	
SyncCtrl	Digital, input	[0] = no sync, [1] = sync PLL re-entry after 'dark' or TxD periods
PLLclkout	Digital, output	System clock 13.56 MHz (PLL generated in 'dark period')
TxD	Digital, input	Active high, RF coil clamped/back-scatter (PLL free running)
TxDsoft	Digital, input	Active high, (Instead of TxD when no PLL and only 10% modulation)
EnaRC	Digital, input	Enable RC oscillator, Active high
RCclkout	Digital, output	RC clock output for household logic, [1] when disabled

Electrical characteristics

Parameter	Conditions	Min	Type	Max	Unit
RF carrier frequency			13.56		MHz
Supply voltage	Regulated supply voltage (VddA)	1.62	1.8	1.98	V
VPOR_th_up	Power-on-reset rising threshold		1.7		
Coil current	Average	0		60	mA
Isupply_RFfrontend	10% or 100% modulation		225		µA
	10% modulation with PLL disabled		100		
Isupply_RFfield[1]	ISO/IEC 14443 at 1.5 A/m		~5		mA
	ISO/IEC 15693 at 0.15 A/m		~500		µA
RC oscillator frequency			32		kHz

[1] Depending on antenna and trimming. Assuming 4 winding ISO standard 7810 card size 0.0046 m^2 with 3.3 µH and 5 Ω