

# SEM analysis reveals real cause of chip failure

*Trouble-shoot problems quickly to save time*

## Introduction

DELTA offers to be your ASIC supplier, designing your device, manufacture the silicon in the Far East, and conduct encapsulation and final testing of the component before delivery of components ready for your production.

## Failure issues

When it comes to ASIC design, DELTA's motto is "first time right". When the first wafers from the wafer fab showed severe electrical malfunction, we were extremely frustrated.

## Failure investigation

Immediately, the design team started electrical characterisation of prototypes. Overall, a short between power and ground was observed and furthermore RF inputs exhibited strange VI characteristics.

The circuit behaviour was analysed in detail. In order to understand the conducted analysis some background information of the circuit design was necessary.

The ASIC was a RFID device.

The actual circuit between RFIN1 and RFIN2 is shown in fig. 1. The ASIC was made in three different design variants, type 1, 2 and X. Note that ESD protection circuit does not exist in type X design. Further the 100 KΩ resistor does not exist in the type 2 design.

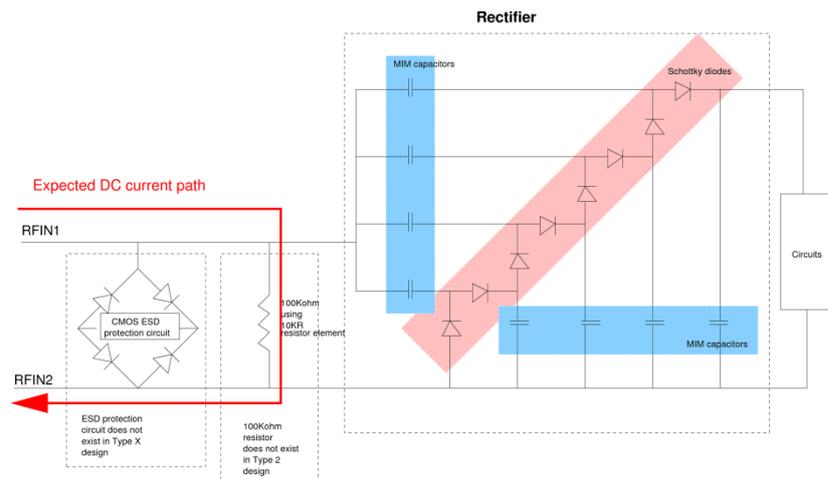


FIG. 1 The circuit between RFIN1 and RFIN2. Modulator and demodulator circuits are not shown for the sake of simplicity.

The circuit between VDD18 and RFIN2 is shown in fig. 2. This part of the design is the same for all three design variants.

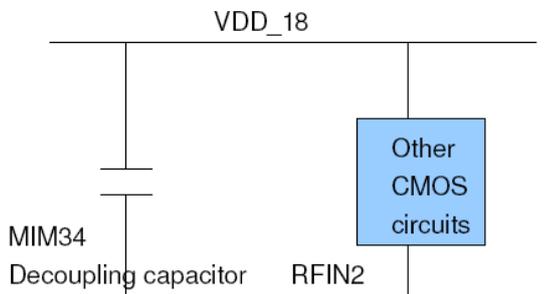


FIG. 2 A drawing of the circuit between VDD\_18 and RFIN2.

The first step of the detailed debugging was to measure the DC-VI curves between RFIN1 and RFIN2 and between VDD18 and RFIN2.

### DC-VI curves between RFIN1 and RFIN2

Based on knowledge of the design, we expected the results to:

- Be the same as that for a 100 KΩ resistor for type 1 and X. Therefore the VI-curve is expected to be a straight line.
- Have high impedance for type 2 as there is no DC path.

The obtained results showed, however, quite a different VI characteristic. All three types showed the same VI-curve which is similar to one of an anti-parallel Schottky diode (see fig. 3).

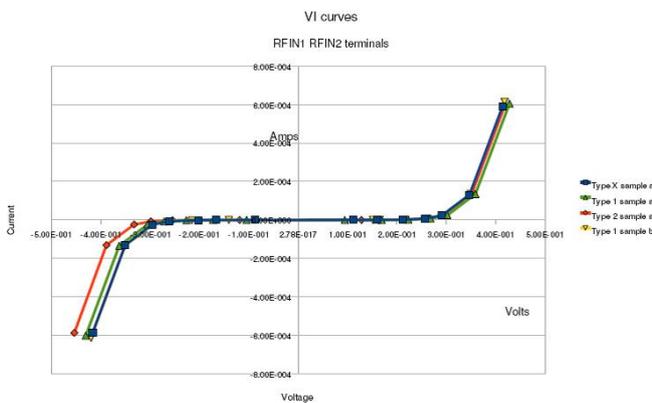


FIG. 3 Obtained VI-curves for the three design variants.

### What if .....

The design team discussed these results and came up with a possible explanation. What if - for some reason - the MIM capacitors are shorted<sup>1</sup>? Then - in this case - the rectifier circuit would transform to anti-parallel Schottky diodes (see fig. 4).

<sup>1</sup> A MIM capacitor is an embedded capacitor, metal-insulator-metal.

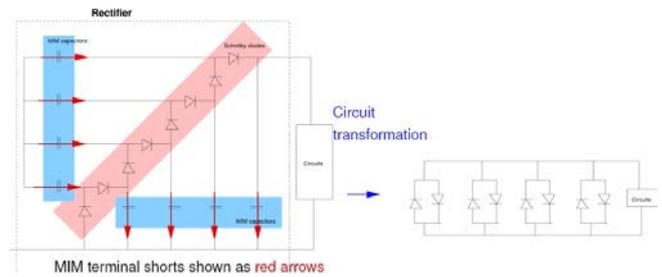


FIG. 4 Shows how the circuit will be if the MIM capacitors are shorted.

A simulation based on this theory was run and resulted in a curve similar to the obtained VI characteristics.

Therefore, shape and magnitude of the curves suggest that MIM caps are shorted.

### DC-VI curves between VDD18 and RFIN2

The expectation was that the DC-VI curves should be the same as between CMOS VDD and GND, i.e.:

- Megaohms in the forward direction
- The parasitic PN diode should dominate the reverse direction.

However, again here the actual results were surprising. For all 3 types the obtained results indicate a short between VDD18 and RFIN2 (see fig. 5).

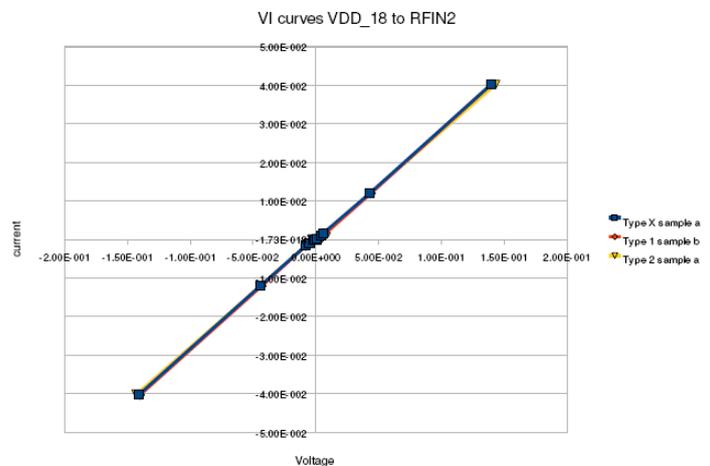


FIG. 5 Obtained VI-curves between VDD18 and RFIN2. Resistance for all three variants is about 3.5 Ω.

Fig. 2 shows that there is a MIM decoupling capacitor between VDD18 and RFIN2. Again a short of this MIM capacitor will explain the obtained results of measurements on the prototypes.

Based on this evaluation, we investigated whether anything had gone wrong in the processing of the MIM capacitors. A review of the design of the capacitor layers showed that all design rules were fulfilled.

One die was then inspected optically but with no indication of process irregularities (see fig. 6).

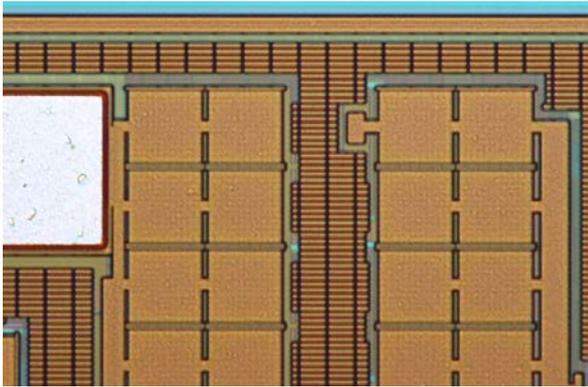


FIG. 6 Optical micrograph showing part of the MIM capacitors.

### Inspection by SEM examination

A quick cross-section through the MIM capacitors was now prepared and subsequently inspected by use of a Scanning Electron Microscope (SEM).

This investigation showed that the top metal layer (metal 4) was slightly misaligned – a little less than 1  $\mu\text{m}$  shift. This small misalignment caused a short in the MIM capacitors as one tungsten via - that should connect to the capacitor top metal - connected to the capacitor bottom layer (metal 3) (see fig. 7).

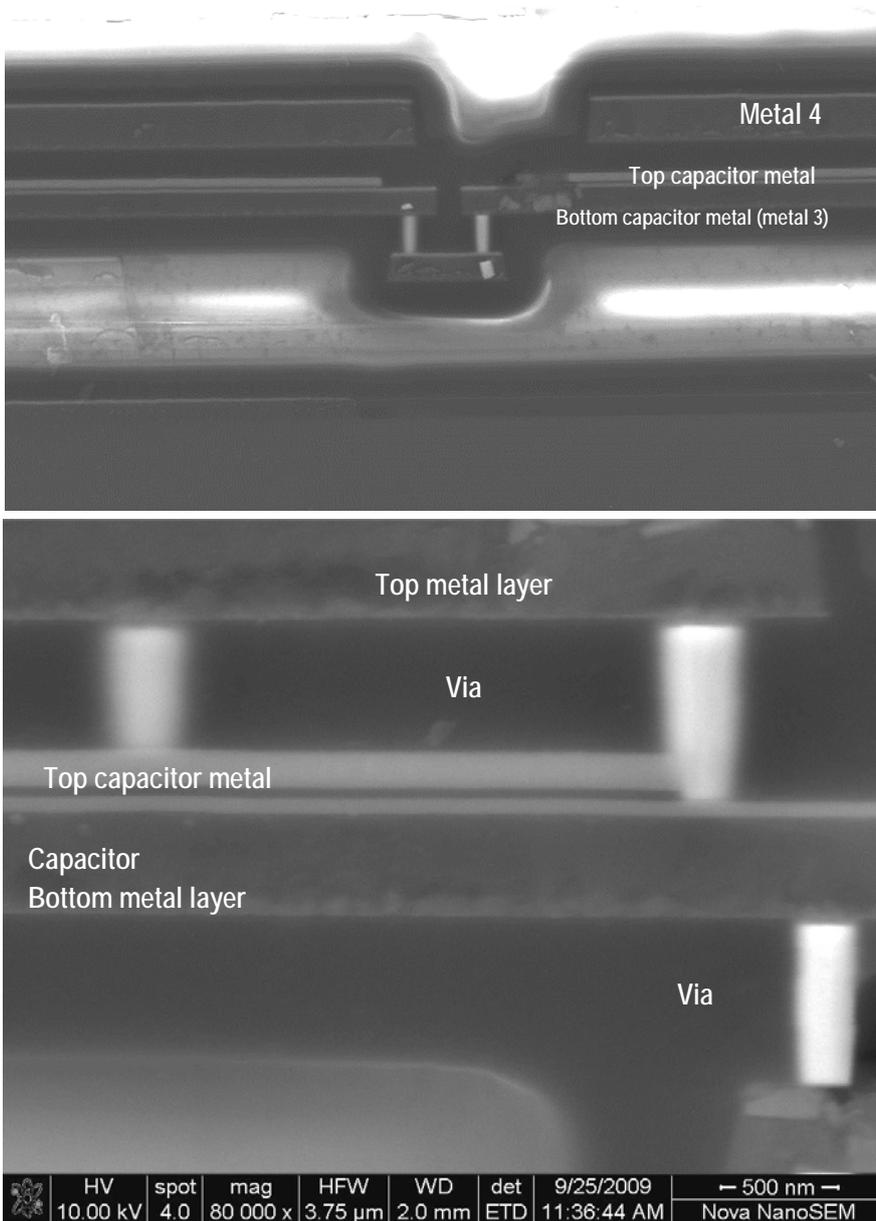


FIG. 7 SEM micrographs showing a cross-section of the MIM capacitor. Upper side view of the centre of the capacitor. The top metal layer is shifted to the right.

The micrograph below is an enlargement of part of the capacitor showing how the outer via is connecting to metal 3 instead of the top capacitor metal, thereby shorting the capacitor.

The small misalignment of metal 4 also explained another issue found during the debug of the prototypes. The performed electrical measurements pinpointed a poly silicon resistor (fig. 1 – type 1 and X) to be open/not processed.

A cross section through the resistor showed that metal 4 had no contact to metal 3 as intended (see fig 8).

### Corrective actions

The results of this SEM evaluation were communicated to the wafer fab who immediately initiated a new wafer run.

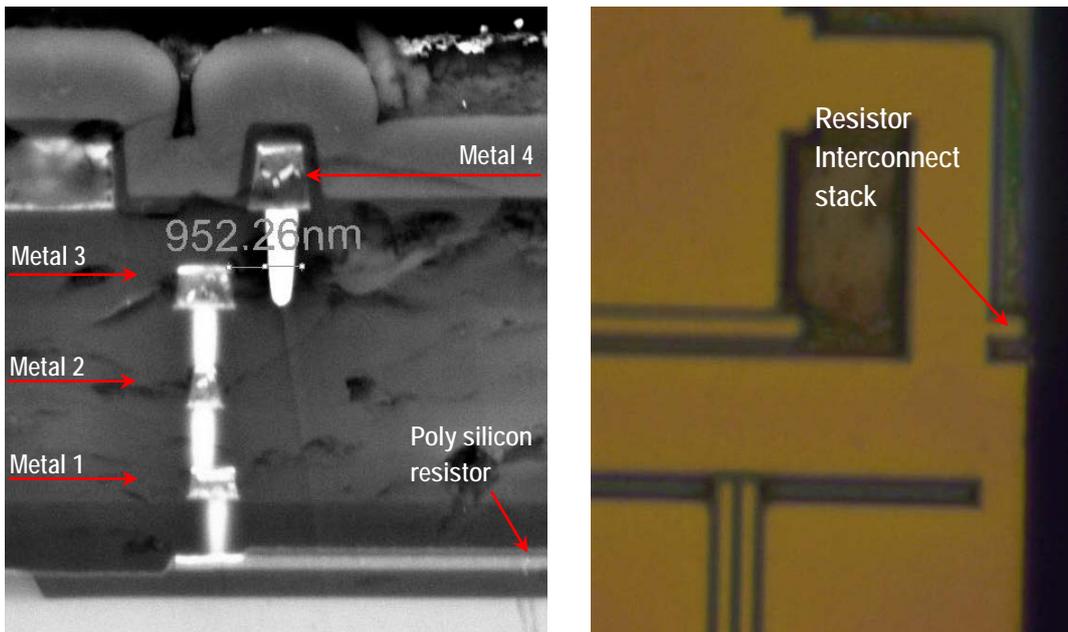


FIG. 8 On the right the position of the cross-section relative to the poly silicon resistor is shown. On the left the missing contact between metal 4 and 3 can be seen on the SEM micrograph.

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