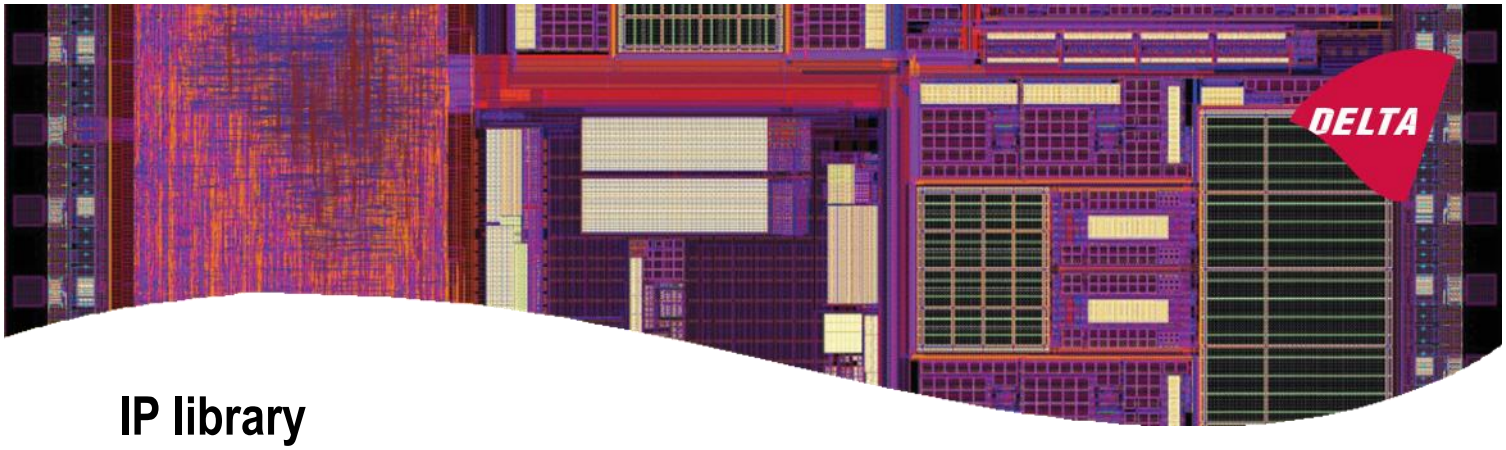

IP library

List of DELTA's Intellectual Properties

Overview

We have based our ASIC designs on the reuse of selected sets of functional blocks, each verified in silicon/FPGA. These blocks can be reassembled in your customised configuration. This approach significantly reduces risk and cost, and shortens time to market. DELTA is continuously expanding our portfolio of IPs in key application areas.

Excerpts from the catalogue

- 8/32 bit processor cores
- UART, IIC Core, USB 1.1
- LVDS I/Os
- DES/3DESS processor
- SHA-1 hash
- HDLC controller (DSRC)
- ADCs 8 – 10 bit, DACs 8 – 10 bit
- 16 bit Sigma Delta ADC
- Bandgap vref.
- Op. amplifiers, instrumentation amps, transconductance amps, Switched CAP amps
- PLLS (32 kHz – 16 MHz)
- Voltage regulators, ULP Voltage regulators
- RC osc. ULP, X-Osc ULP, POR and Brown Out Detectors
- Photodiode sensor based on standard CMOS Process
- Hall effect sensors
- DSRC analog front-end & baseband
- RFID 14443/15693 analog front-ends
- RFID 14443/15693 modulator/demodulator
- EPC GEN2 front-end (UHF RFID) (in development)
- EPC GEN2 modulator/demodulator

Analog / mixed signal design

- Ultra low power/low voltage analog/mixed signal design
- Block level simulation, post layout simulation, modelling (Verilog A)
- Sub-threshold design (weak inversion)
- Chip architecture (power supplies, Power On Reset, pads, floorplan, power distribution, substrate)
- Design/layout for low noise considerations
- Test harness design
- Layout at block and chip level
- LVS & DRC

Digital design

- Digital IC design and verification
- RTL coding (VHDL, Verilog)
- Synthesis
- System integration of 3rd party
- IPs, ROM, RAM, EEPROM, OTP
- DFT methodology (JTAG, BIST, Scan Insertion)
- Clock tree insertion
- Floorplanning (power distribution, IR-drop)
- Place & Route
- Static Timing Analysis
- LVS & DRC

Verification / Test

- Mixed signal verification at chip level (VHDL/Verilog, RTL, Verilog-AMS, Spice)
- Scripted simulations for regression testing
- Scripted corner / Monte Carlo simulations
- Equivalence checking
- ATPG, production test vector generation
- Test program development for production testing
- Failure analysis capabilities in-house

Delivery of components

- Prototype assembly in-house
- Packaging of components
- Qualification testing (HTOL, ESD, Burn-in)
- Volume production testing in-house (packaged or at wafer level
- Yield analysis and optimisation

DELTA · Venlighedsvej 4 · 2970 Hørsholm · Denmark - Tel. (+45) 72 19 40 40 · asic@delta.dk · asic.madebydelta.com

NanoComplete

DELTA can, in cooperation with our partner, Sondrel, offer total solutions for SoC type designs in deep submicron processes targeting the complex and high speed SoC application area.

Technologies

- CMOS 0.8 µ to 0.18 µ and beyond
- BICMOS

Tools

- CADENCE (Analog, Digital, Mixed Signal and Encounter P&R)
- MatLab incl. Simulink
- Modelsim
- Synopsys synthesis
- Mentor Graphics DftAdvisor, FastScan and FlexTest
- Calibre LVS&DRC
- Verigy 93000 RF and high pin-count testers (2 pcs.)
- Verigy 83000 digital tester
- Teradyne Catalyst mixed signal tester
- Teradyne A585 mixed signal tester
- Teradyne J750 digital tester
- X-ray, SEM and more for failure analysis. Access to FIB
- Wire bonding and flip chip for prototype assembly

Key applications

- DSRC Toll road transponders
- RFID tags for niche applications (privacy functions, connected health applications, sensor interfaces etc.)
- Ultra low power/low voltage battery operated sensor interface devices
- Optical sensor applications
- Retarget of (standard) components to ASICs

For further information please contact us

asic@delta.dk